Leakage Reduction in Sub-threshold FPGAs

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ECE 6332 Final Presentation

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Outline

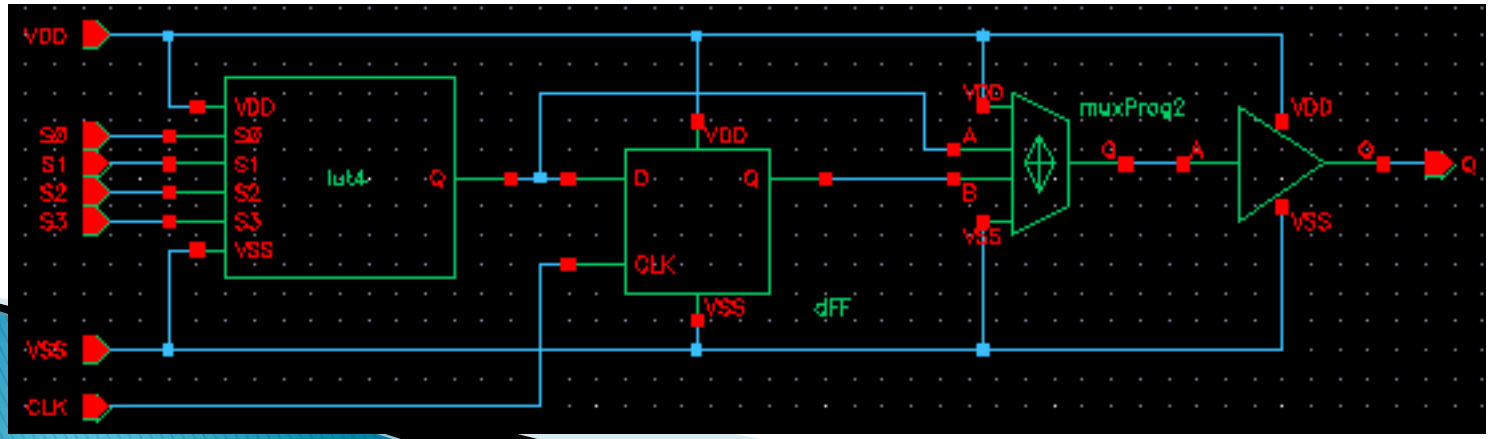
- FPGA Overview
- Project Overview
- Leakage Reduction Analysis
- Concluding Remarks
- Future Work

FPGA Overview

- Logic, switch, I/O blocks, interconnect
- Advantages
  - Flexible, widely applicable, reconfigurable
  - Low non-recurring engineering costs
- Disadvantages
  - Increased complexity vs. ASICs
  - Increased Complexity = Increased Energy
- Sub-threshold operation = Reduced energy

Project Overview

- Leakage major factor in sub-threshold
- What reduction methods most effective?
- Focused on SRAM-based CLB architecture
  - 16 programmed muxes per CLB
  - 4 BLEs per CLB
  - 1 DFF, 4-input LUT, 2-input mux per BLE



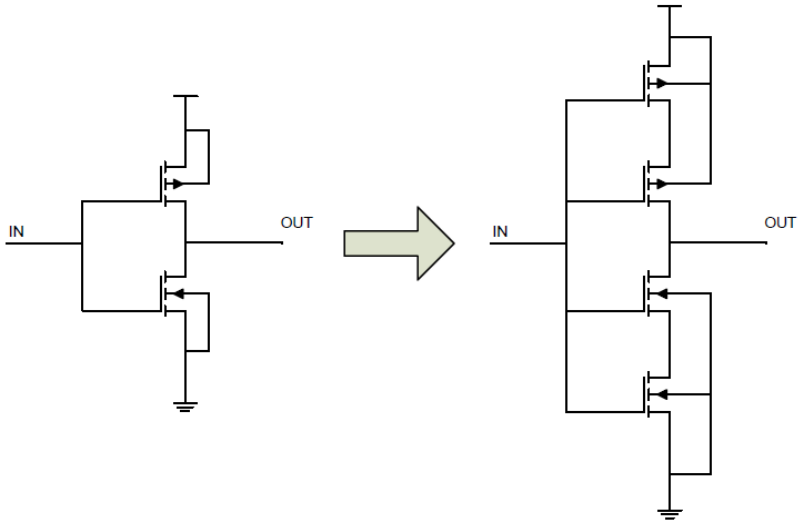
Project Overview

- In total:
  - 328 SRAM cells
  - 400 Transmission Gates
  - 172 Inverters
- 2 configurations: 2, 4 series inverters
- Base characteristics at 300mV:
  - Total Delay: 156 ns
  - Total Energy: 46.9 pJ
  - Leakage Energy: 38.5 pJ
  - Leakage Current: -771nA

Leakage Reduction Methods

- Four leakage methods tested
  - Stacking
  - Dual-Vt architecture
  - Sub-threshold-specific body biasing
  - MTCMOS architecture

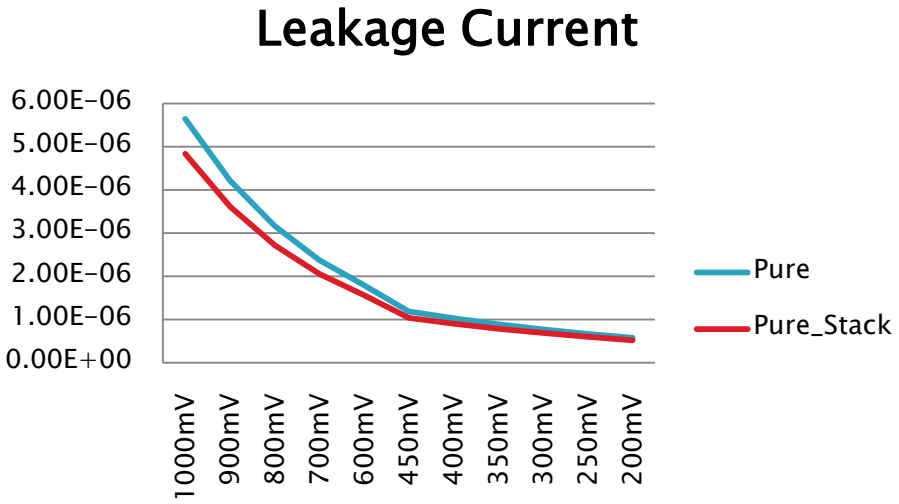
Stacking



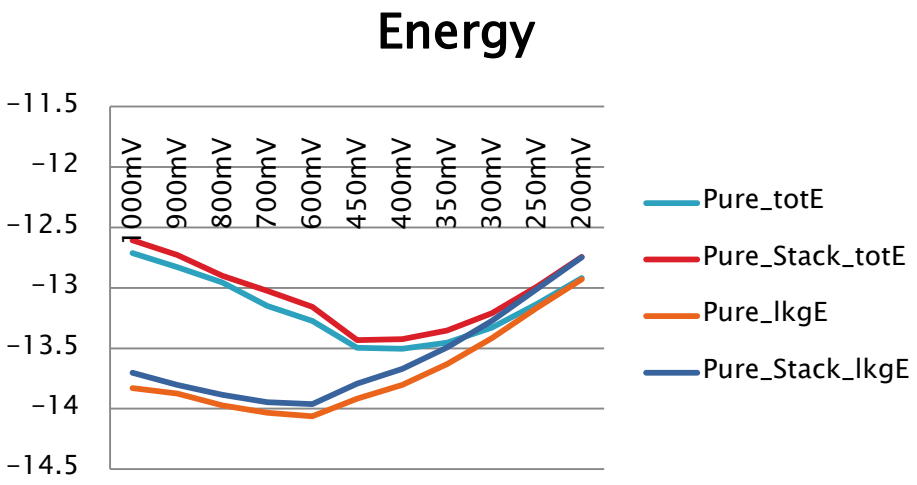
Reduce Leakage current for 3 reasons:

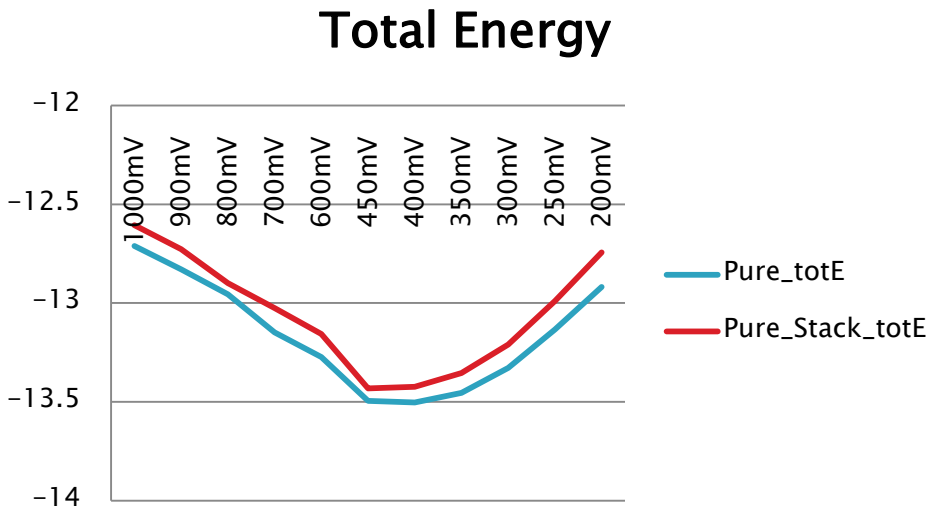
1. Decrease V_{GS}
2. Body biasing
3. DIBL

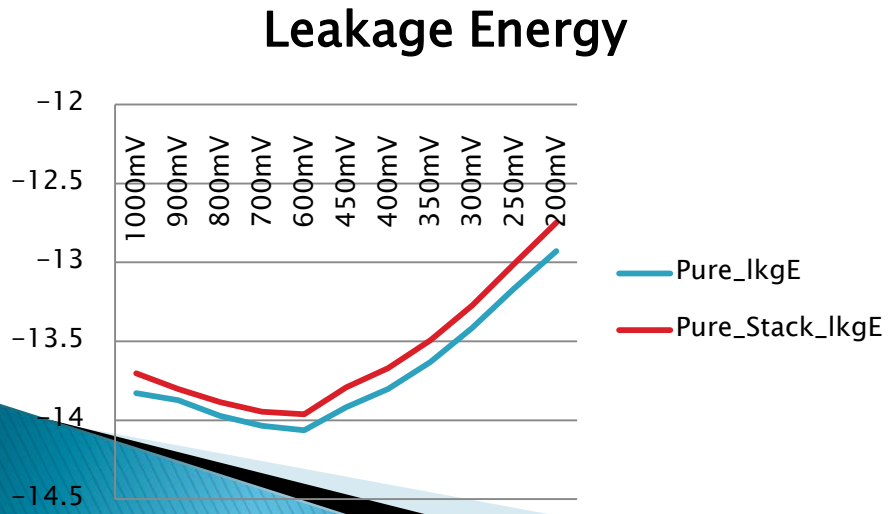
Stacking every inverter in the FPGA

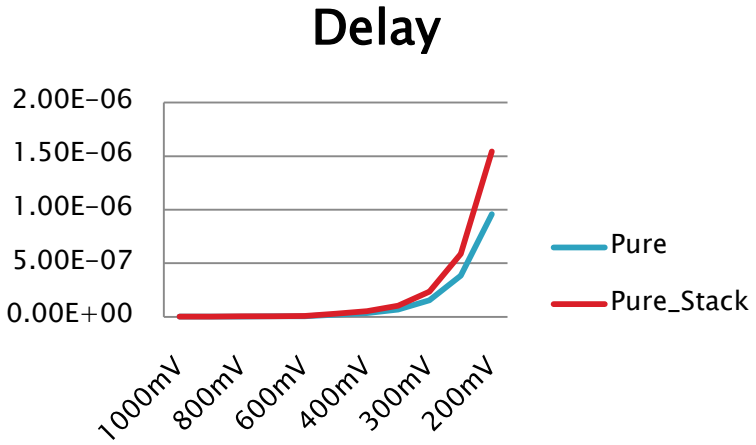


Stacking


Energy
-11.5
-12
-12.5
-13
-13.5
-14
-14.5
1000mV
900mV
800mV
700mV
600mV
450mV
400mV
350mV
300mV
250mV
200mV
Pure_totE
Pure_Stack_totE
Pure_lkgE
Pure_Stack_lkgE


Total Energy
-12
-12.5
-13
-13.5
-14
1000mV
900mV
800mV
700mV
600mV
450mV
400mV
350mV
300mV
250mV
200mV
Pure_totE
Pure_Stack_totE


Leakage Energy
-12
-12.5
-13
-13.5
-14
-14.5
1000mV
900mV
800mV
700mV
600mV
450mV
400mV
350mV
300mV
250mV
200mV
Pure_lkgE
Pure_Stack_lkgE

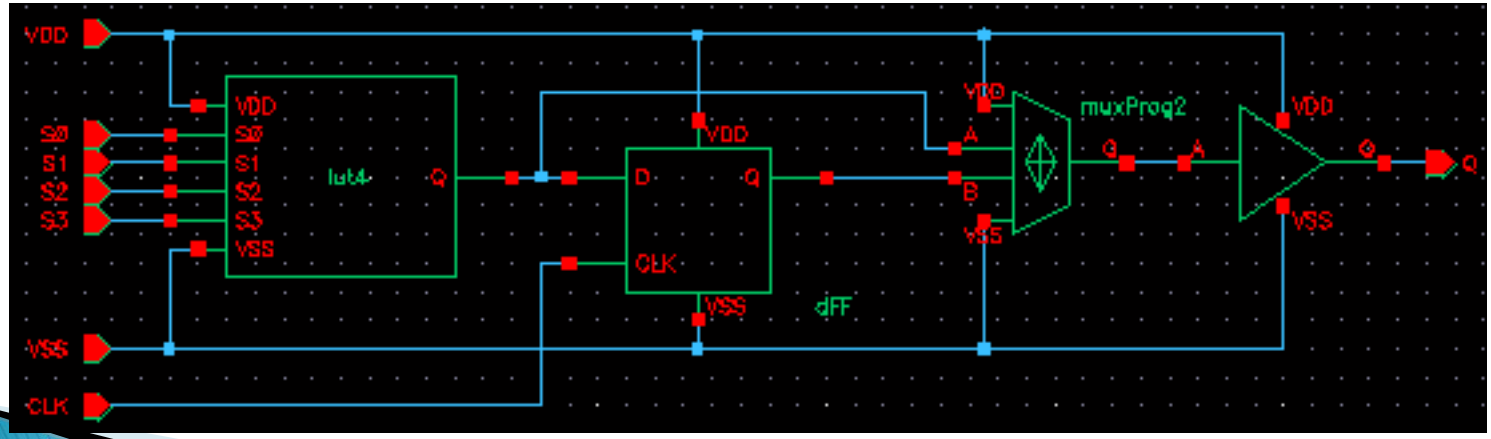

Delay
2.00E-06
1.50E-06
1.00E-06
5.00E-07
0.00E+00
1000mV
800mV
600mV
400mV
300mV
200mV
Pure
Pure_Stack

Dual-Vt

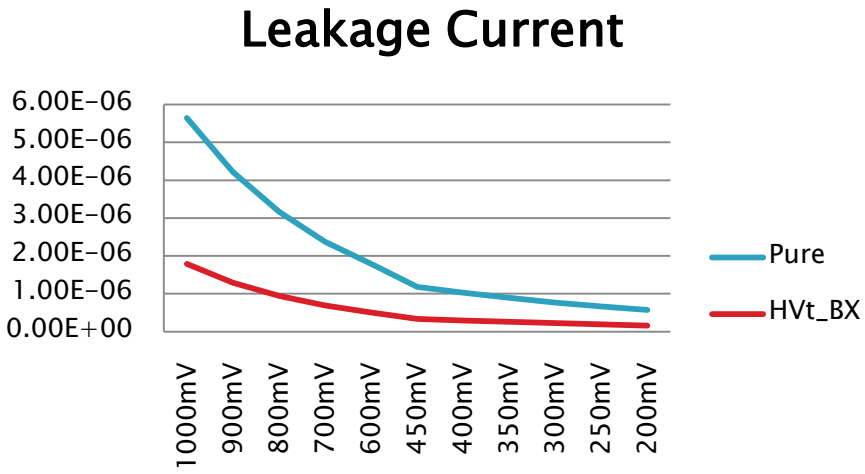
Basic Idea:

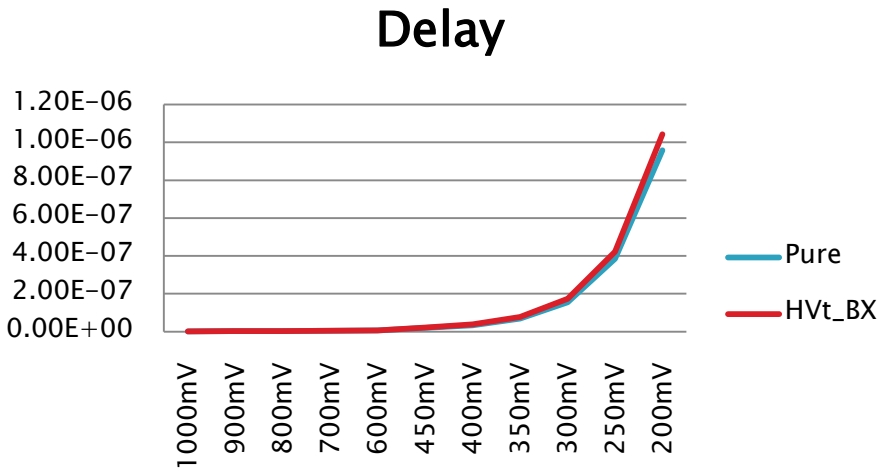
Low Vt in critical path --- maintain speed
High Vt in other part ---- reduce leakage

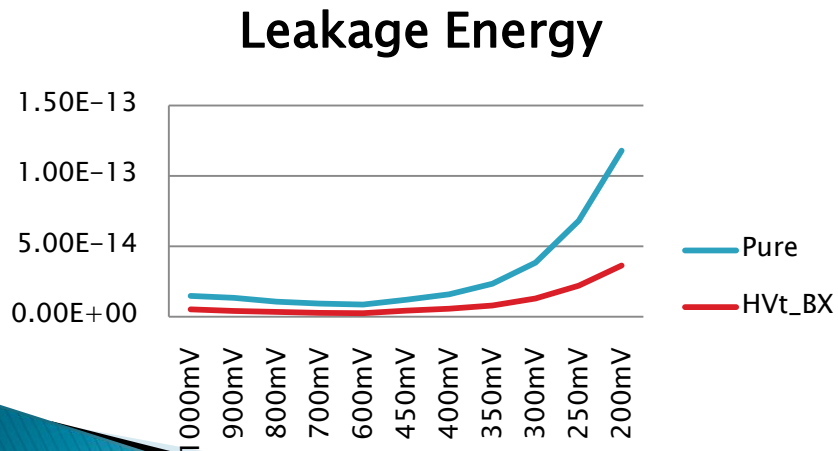
Which path is critical in a FPGA?

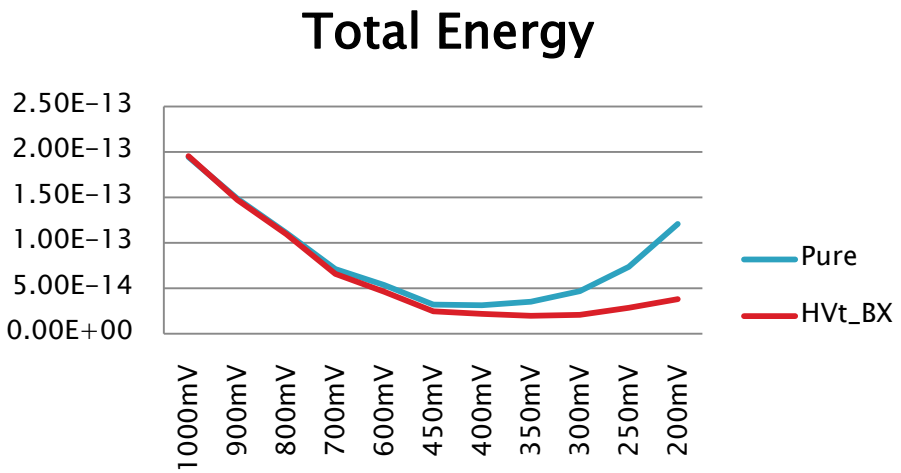


Dual-Vt: H_{Vt} SRAM cell







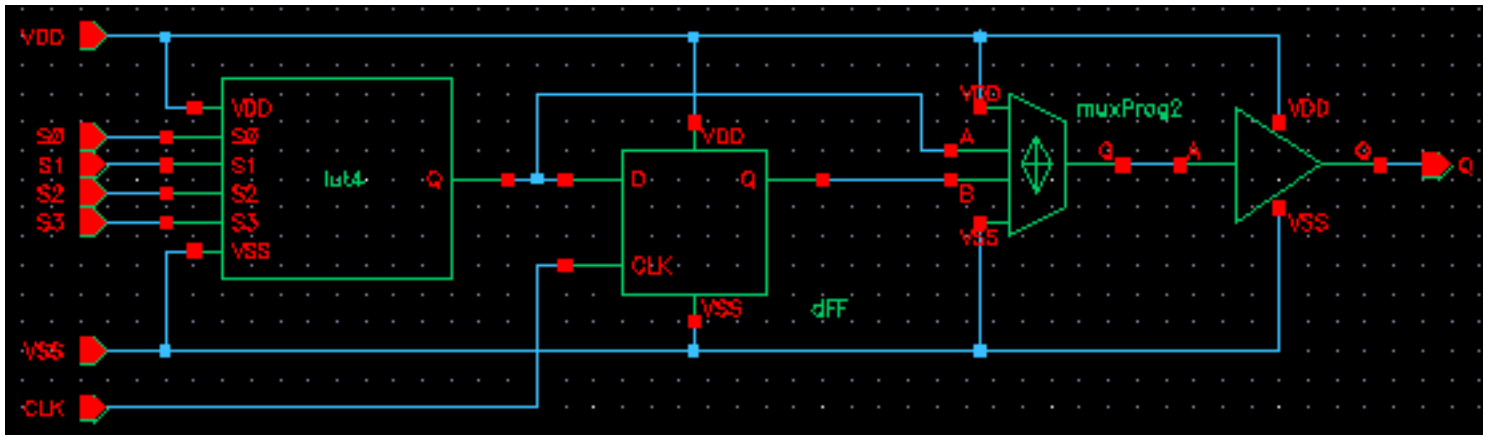


MTCMOS

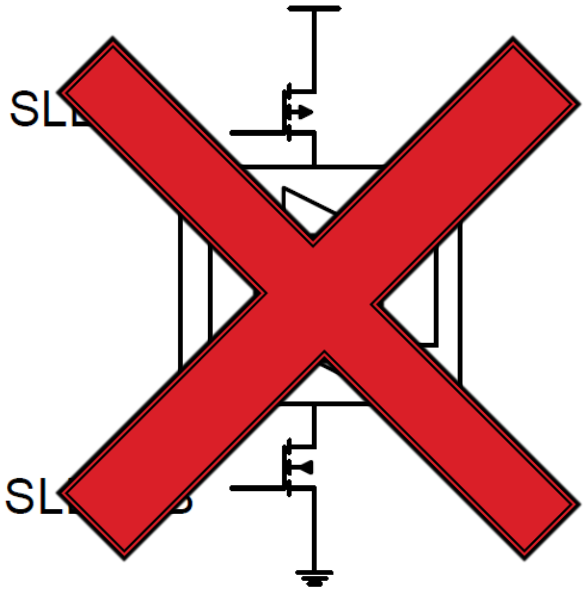
Basic Idea:

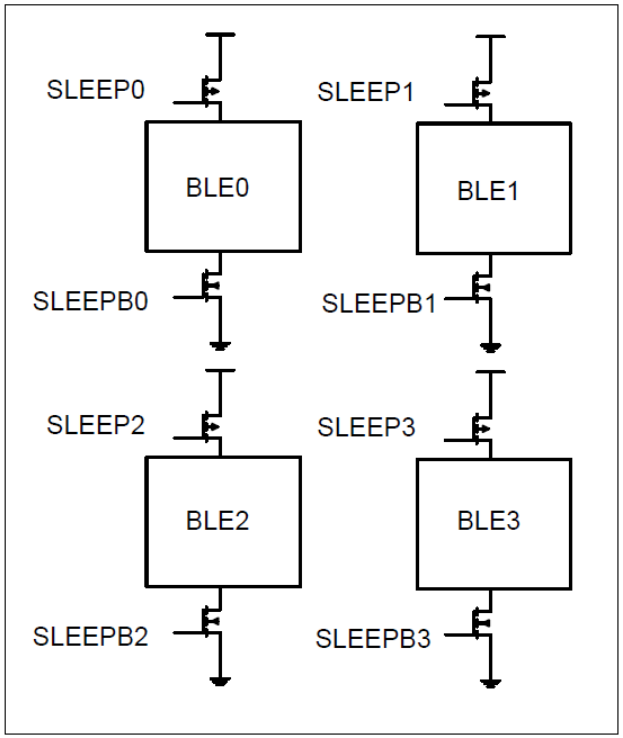
Put blocks in sleep mode when not in use

Which transistors can be turned off?



MTCMOS



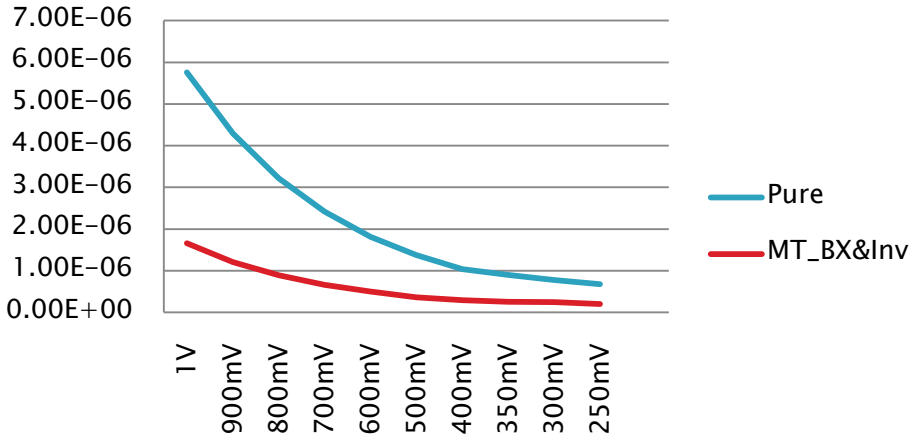


Normal Circuit

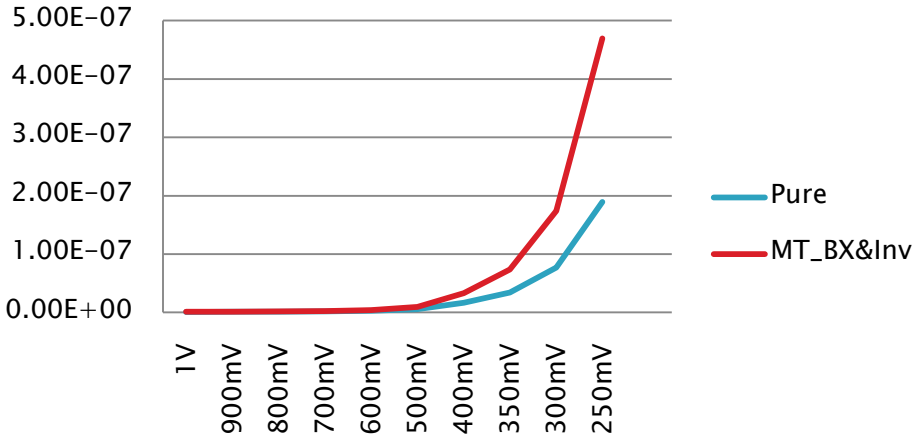
FPGA

MTCMOS

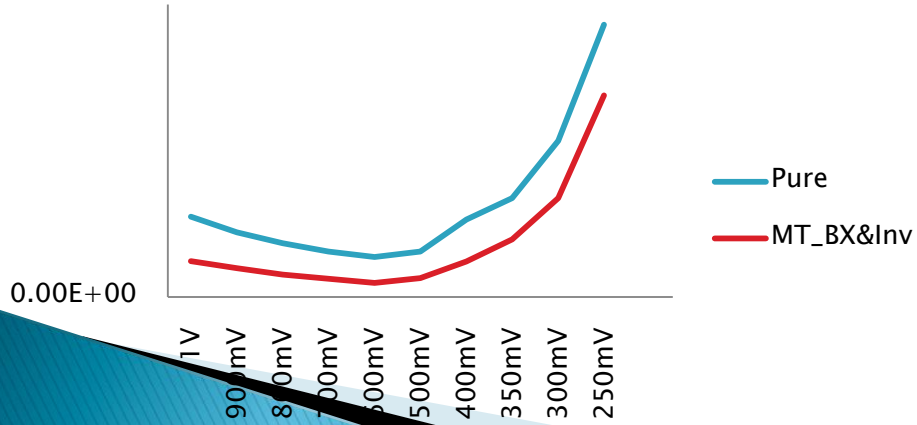
Leakage Current



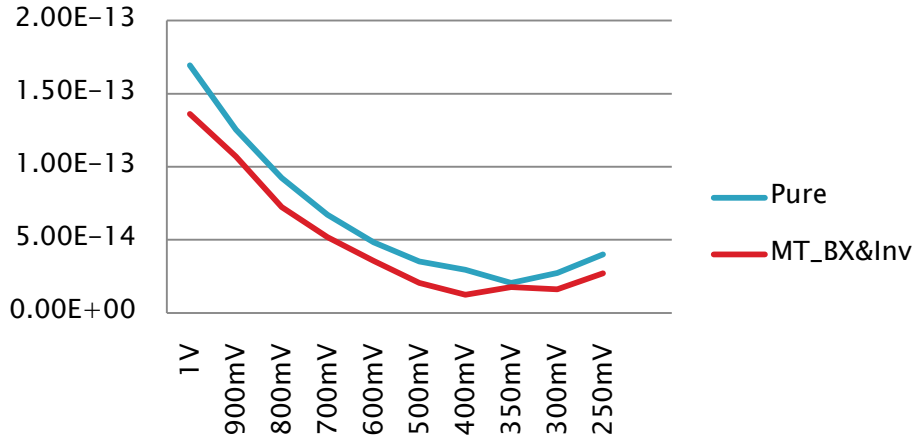
Delay



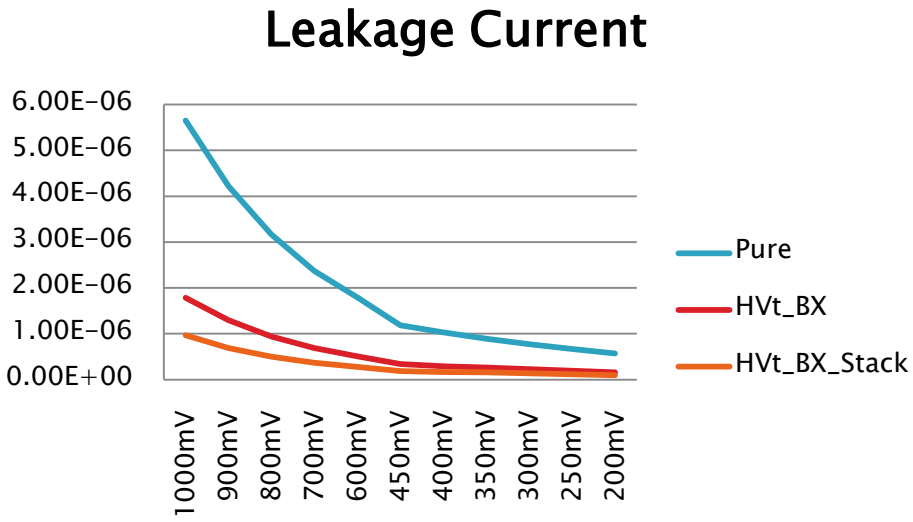
Leakage Energy

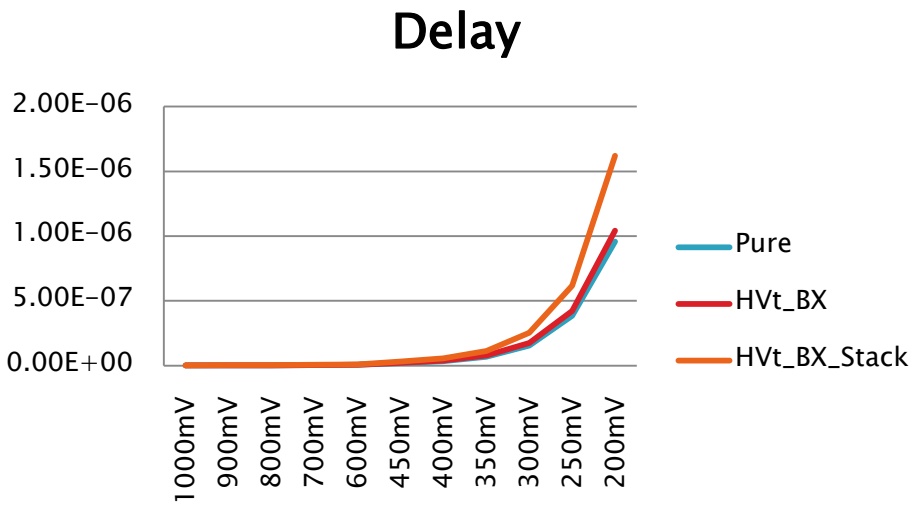


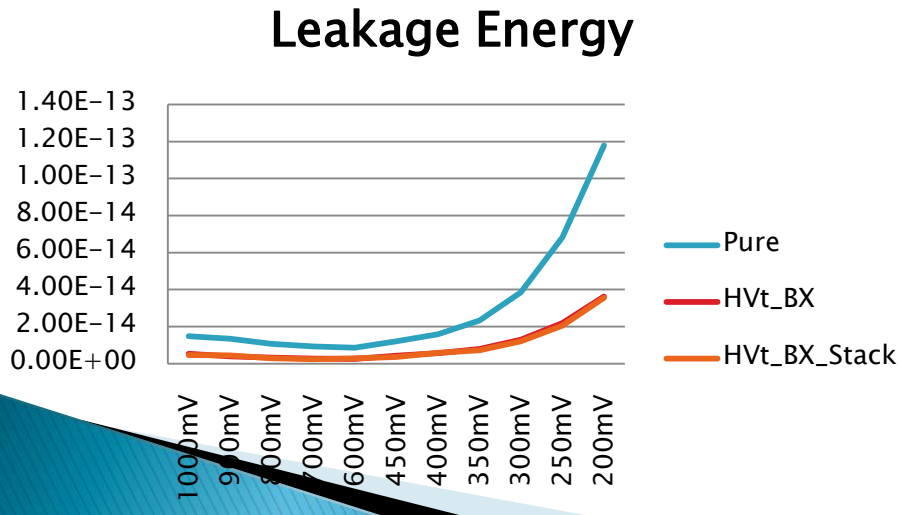
Total Energy

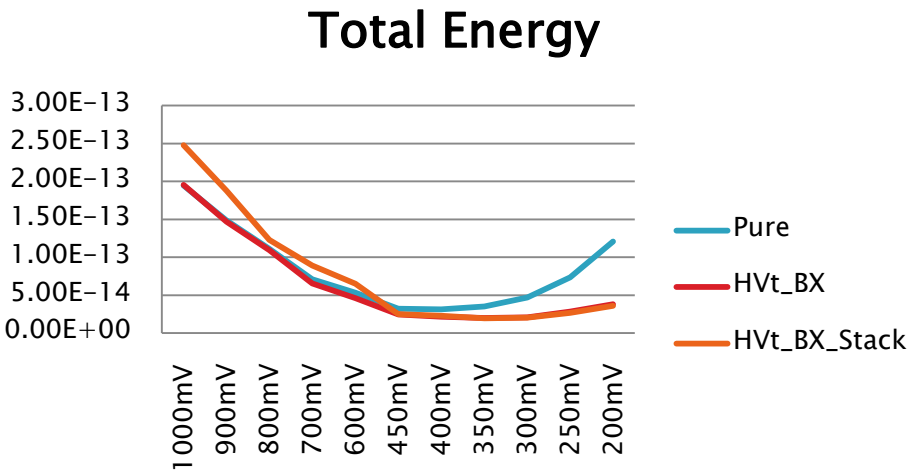


Put it together: Stacking & Dual-Vt



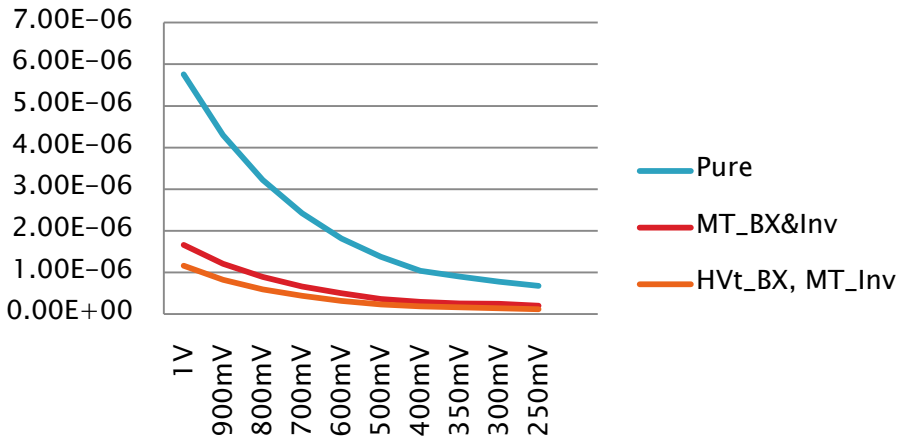




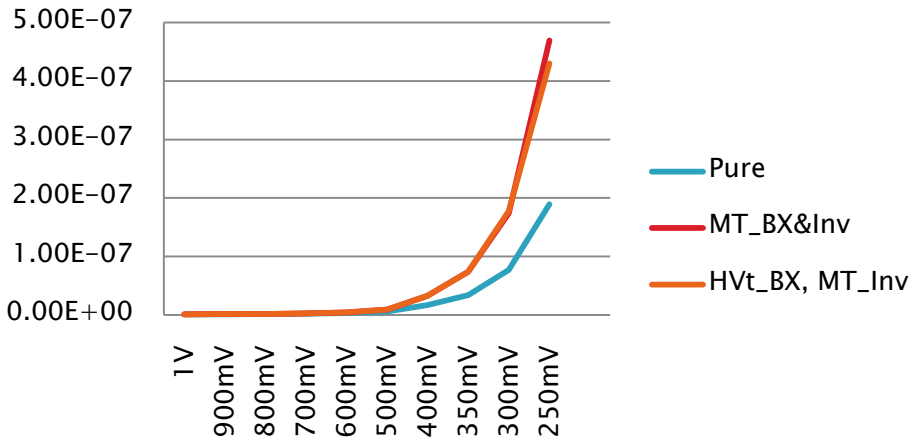


Put it together: MTCMOS & Dual-Vt

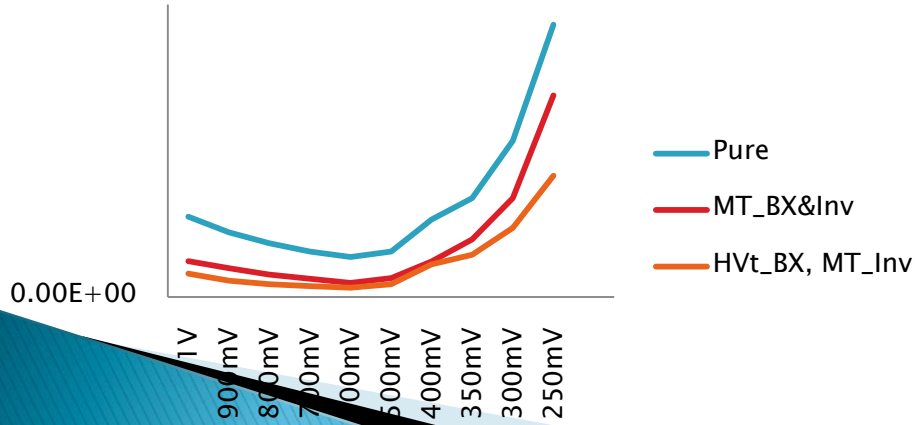
Leakage Current



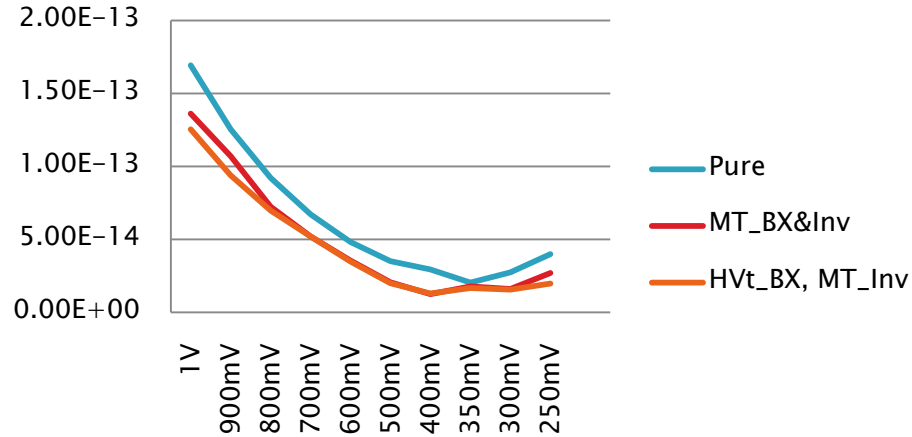
Delay



Leakage Energy



Total Energy



Other methods: Body Biasing

- Connect body to opposite rail
- Advantages:
  - Reduces delay
  - No added area cost
  - Easy to integrate with other methods
- Disadvantages:
  - Increased leakage
  - Could destroy device in super-threshold
- No significant improvement observed

Summary

- Energy limits FPGA applications
- Leakage comprises most sub-Vt energy
- Not all methods worthwhile in FPGA
- MTCMOS, Dual-Vt SRAM most effective
- Configuration vs. Runtime considerations

Future Work

- Optimize other FPGA components
  - Interconnect
  - Clock networks
- Optimize overall FPGA architecture
- Optimize for both configuration, runtime
- Analyze other FPGA configurations

Questions?